EPC23102 and EPC23104 Integrated Circuit Qualification Report

Dr. Shengke Zhang, VP of Reliability, Efficient Power Conversion

November 18, 2025

This report summarizes the Product Qualification results for EPC part numbers EPC23102 and EPC23104 which meets all required qualification requirements and is released for production.

Scope

The testing matrix in this qualification report covers the qualification tests performed on EPC23102 and EPC23104 for the component-level qualification. EPC23102 is a 100 V, 35 A and EPC23104 is a 100 V, 15 A half-bridge power stage, comprised of two eGaN FETs and 5 V logic integrated gate-driver in a QFN package with exposed backside silicon substrate.

Part Number	Package Size (mm x mm)
EPC23102	L (3.5 x 5)
EPC23104	L (3.5 x 5)

Qualification Test Overview

Devices of EPC23102 and EPC23104 were subject to a wide variety of stress tests, according to JEDEC standard JESD47L[1]. The stress tests include the following:

- High Temperature Operating Life (HTOL): Parts are subjected to recommended operating conditions at T_J = 125°C for 1000 hours.
- High Temperature Humidity Bias (THB): Parts are subjected to ambient temperature of 85°C and 85% relative humidity (RH), with a constant V_{IN} voltage (80 V), V_{DRV} voltage (5.5 V), and V_{IN} logic input (0 V).
- High Temperature Storage Life (HTSL): Parts are subjected to a bake at 150°C for 1000 hours.
- Preconditioning (PC): Parts undergo the following steps in sequence: (1) 125°C bake for a minimum of 24 hours; (2) Moisture Sensitivity Level 1 (MSL1) conditions (see MSL1 details below); (3) three times reflow.
- Temperature cycling (TC): Parts are subjected to alternating low and high temperature extremes from -40°C to +125°C for a total of 1000 cycles.
- MSL1: Parts are subjected to moisture, temperature, and three cycles of reflow. MSL1 is the most stringent of the moisture sensitivity levels, requiring 85°C and 85% humidity for 168 hours.
- Electrostatic Discharge (ESD) Characterization: Parts are tested under both Human Body Model (HBM) and Charge Device Model (CDM) to assess device susceptibility to electrostatic discharge events.

All devices tested in this qualification underwent external visual inspection. Damaged parts were removed from the test population.

Parametric measurements were performed at 25°C on all the samples before and after the stress tests to verify compliance with the specifications listed on the product datasheet. The parameters measured include quiescent and operating currents of the driver (V_{DRV}/V_{BOOT} pins), undervoltage lockout (UVLO V_{DRV}/V_{BOOT} pins), input threshold voltages & hysteresis for the logic input signal (V_{IN} High Side (HS)/Low Side (LS) pins), and DC static parameters of the output transistors.

For all the qualification tests except TC, parts were mounted onto high T_g FR-4 adaptor cards with four layers and 1.6 mm in thickness. Type-4 SAC305 solder paste with water-soluble (W/S) flux was used for mounting the parts onto the adapter cards. After assembly, flux residue was cleaned using deionized (DI) water.

High Temperature Operating Life

Parts were subjected to the maximum recommended operating voltages and temperature for a stress period of 1000 hours. The test was conducted in accordance with JESD22-A108[2].

Stress Test	Part Number	Package Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTOL	EPC23102	L (3.5 x 5)	T_J = 125°C, V_{D-D} = 5.5 V V_{IN_DC} = 80 V, Duty Cycle = 50% $V_{IN(HS/LS)}$ = 5 V_{P-P} (Buck Converter Capacitive Load; frequency = 500 kHz)	0	77 x 3	1000
HTOL	EPC23102	L (3.5 x 5)	T_J = 125°C, V_{D-D} = 5.5 V V_{IN_DC} = 80 V, Duty Cycle = 25% $V_{IN(HS/LS)}$ = 5 V_{P-P} (Buck Converter Capacitive Load; frequency = 500 kHz)	0	77 x 1	1000
HTOL	EPC23104	L (3.5 x 5)	T_J = 125°C, V_{D-D} = 5.5 V V_{IN_DC} = 80 V, Duty Cycle = 50% $V_{IN(HS/LS)}$ = 5 V_{P-P} (Buck Converter Capacitive Load; frequency = 500 kHz)	0	77 x 2	1000

Table 1. High Temperature Operating Life Test

Temperature Humidity Bias

Parts were subjected to the maximum recommended operating voltage at 85°C and 85% relative humidity for a stress period of 1000 hours. High-side and Low-side power FETs were stressed independently with V_{IN_DC} = 80 V and V_{SW_DC} = 0 V or V_{IN_DC} = V_{SW_DC} = 80 V, $V_{IN(HS/LS)}$ = 0 V and V_{DRV} = 5.5 V. Stress testing was conducted in accordance with JESD22-A101[3].

Stress Test	Part Number	Package Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
THB	EPC23102	L (3.5 x 5)	T_A = 85°C, RH = 85%, V_{DD} = 5.5 V V_{IN_DC} = V_{SW_DC} = 80 V, $V_{IN(HS/LS)}$ = 0 V	0	25 x 3	1000
THB	EPC23102	L (3.5 x 5)	T_A = 85°C, RH = 85%, V_{DD} = 5.5 V V_{IN_DC} = 80 V, V_{SW_DC} = 0 V, $V_{IN(HS/LS)}$ = 0 V	0	25 x 3	1000
THB	EPC23104	L (3.5 x 5)	T_A = 85°C, RH = 85%, V_{DD} = 5.5 V V_{IN_DC} = V_{SW_DC} = 80 V, $V_{IN(HS/LS)}$ = 0 V	0	25 x 2	1000
THB	EPC23104	L (3.5 x 5)	T_A = 85°C, RH = 85%, V_{DD} = 5.5 V V_{IN_DC} = 80 V, V_{SW_DC} = 0 V, $V_{IN(HS/LS)}$ = 0 V	0	25 x 2	1000

Table 2. Temperature Humidity Bias Test

High Temperature Storage Life

Parts from EPC23102 and EPC23104 were subjected to an ambient temperature of 150°C for a total duration of 1000 hours.

Stress Test	Part Number	Package Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTS	EPC23102	L (3.5 x 5)	T_A = 150°C Air, Unbiased	0	25 x 3	1000
HTS	EPC23104	L (3.5 x 5)	T_A = 150°C Air, Unbiased	0	25 x 2	1000

Table 3. High Temperature Storage Test

Temperature Cycling

Parts were subjected to temperature cycling (TC) between -40°C and 125°C for a total duration of 1000 cycles. In accordance with JEDEC Standard JESD22-A104[4], 10 minutes dwell time was used in the hot and cold temperature extremes and heating/cooling rates were approximately 15°C per minute. Loose sample parts were placed in a tray during the TC test.

Stress Test	Part Number	Package Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Cys)
TC	EPC23102	L (3.5 x 5)	T_A = -40°C to +125°C	0	25 x 3	1000
TC	EPC23104	L (3.5 x 5)	T_A = -40°C to +125°C	0	25 x 2	1000

Table 4. Temperature Cycling Test

Moisture Sensitivity Level 1

Parts were subjected to MSL1 conditions in accordance with the IPC/JEDEC joint Standard J-STD-020[5] for Pb-free solder.

Stress Test	Part Number	Package Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
MSL1	EPC23102	L (3.5 x 5)	T_A = 85°C, RH = 85% 3x reflow	0	25 x 9	168
MSL1	EPC23104	L (3.5 x 5)	T_A = 85°C, RH = 85% 3x reflow	0	25 x 6	168

Table 5. Moisture Sensitivity Level Test

Electrostatic Discharge (ESD) Sensitivity

EPC23102 and EPC23104 was subjected to ESD sensitivity test using both the human body model (HBM) and charged device model (CDM). Testing was conducted according to JS-001-2023[6] and JTR002-01-22[7] JEDEC standard. EPC23102 and EPC23104 passed the HBM and CDM tests with a rating of ±500 V.

Stress Test	Part Number	Package Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)
ESD-HBM	EPC23102	L (3.5 x 5)	±500 V	0	3 x 1
ESD-CDM	EPC23102	L (3.5 x 5)	±500 V	0	3 x 1
ESD-HBM	EPC23104	L (3.5 x 5)	±500 V	0	3 x 1
ESD-CDM	EPC23104	L (3.5 x 5)	±500 V	0	3 x 1

Table 6. Electrostatic Discharge (ESD) Sensitivity

[1] JESD47L, "Stress-Test-Driven Qualification of Integrated Circuits", December 2022
[2] JESD22-A108, " Temperature, Bias, and Operating Life", December 2022
[3] JESD22-A101, "Steady-State Temperature-Humidity Bias Life Test", January 2021
[4] JESD22-A104, "Temperature cycling", April 2023
[5] J-STD-020F, "Moisture/Reflow Sensitivity Classification for Non-hermetic Surface Mount Devices (SMDs)", December 2022
[6] JS-001-2023, "Human Body Model (HBM) Component Level", July 2023
[7] ESDA/JEDEC JTR002-01-22, "Charged Device Model Testing of Integrated Circuits", December 2022